CLAIMS

What is claimed is:

1. A chip scale package carrier for electrically connecting an integrated circuit die with ground connections and bond wire signal connections to a primary circuit board, said carrier comprising:

a plurality of wire bond fingers on a top side of said carrier to receive bond wires attached to respective ones of the signal connections on the die;

a first plurality of solder ball pads on a bottom side of said carrier electrically coupled to said wire bond fingers on said top side;

a first ground plane disposed on said top side of said carrier, said first ground plane surrounding said plurality of wire bond fingers and covering a die mounting area on said top side of said carrier;

a second ground plane disposed on said bottom side of said carrier, said second ground plane covering a central area of said bottom side of said carrier, with said first plurality of solder ball pads arrayed generally around said second ground plane;

a plurality of thermal vias electrically and thermally coupling said first and second ground planes; and

a second plurality of solder ball pads on said bottom side of said carrier, said second plurality of solder ball pads formed within said second ground plane.

2. The chip scale package carrier of claim 1 further comprising a plurality of signal vias electrically coupling said plurality of wire bond fingers and said first plurality of solder balls.

3. The chip scale package carrier of claim 2 wherein said plurality of signal vias and said plurality of wire bond fingers comprise combined groups of said wire bond fingers and said signal vias generally distributed around said die mounting area of said top side of said carrier.

4. The chip scale package carrier of claim 3 wherein a portion of said first ground plane covering said die mounting area comprises a hatched ground plane.

5. The chip scale package carrier of claim 1 further comprising:

a first set of solder balls, respective ones of said first set of solder balls coupled to respective ones of said first plurality of solder ball pads; and

a second set of solder balls, respective ones of said second set of solder balls coupled to respective ones of said second plurality of solder ball pads;

said first and second sets of solder balls operative to attach said chip scale carrier package to the primary circuit board.

6. A chip scale package assembly comprising:

an integrated circuit die having bond wires for electrically interconnecting with said die;

a carrier for electrically interconnecting said die with a primary circuit board, said carrier comprising:

a substrate comprising top and bottom sides, said top side comprising a die mounting area to receive said die;

wire bond fingers on said top side of said substrate to receive said bond wires from said die;

signal pads on said bottom side of said substrate electrically coupled to said wire bond fingers;

a first ground plane generally covering said top side of said substrate but leaving exposed said wire bond fingers;

a second ground plane generally covering a central area of said bottom side of said substrate, said signal pads generally arrayed about said second ground plane;

ground pads on said bottom side of said substrate, said ground pads positioned within and electrically coupled to said second ground plane; and

thermal vias positioned within said die mounting area thermally and electrically coupling said first and second ground planes.

7. The chip scale package assembly of claim 6 further comprising a plurality of signal vias extending through said substrate to provide said electrical coupling between said wire bond fingers and said signal pads.

8. The chip scale package assembly of claim 7 wherein said wire bond fingers and said plurality of signal vias are arranged in combined groups of wire bond fingers and corresponding signal vias, said combined groups generally positioned along top-side edges of said substrate.

9. The chip scale package assembly of claim 8 wherein said first ground plane comprises a continuous ground plane surrounding each said combined group of said wire bond fingers and said corresponding signal vias.

10. The chip scale package assembly of claim 6 wherein a portion of said first ground plane within said die mounting area comprises a hatched ground plane.

11. The chip scale package assembly of claim 6 wherein said die further comprises at least one ground connection to electrically couple with said first ground plane covering said die mounting area of said top side of said substrate.

12. The chip scale package assembly of claim 6 further comprising a plurality of solder balls attached to said signal and ground pads on said bottom side of said substrate operative to electrically and thermally couple said die to the primary circuit board.

13. A chip scale package carrier for electrically and thermally coupling an integrated circuit die having bond wire signal connections and at least one ground connection to a primary circuit board, said carrier comprising:

a mounting area on a top side of said carrier to receive the die;

a plurality of wire bond fingers on said top side of said carrier to receive bond wires interconnecting the signal connections on the die with respective ones of said plurality of wire bond fingers;

a plurality of signal pads on a bottom side of said carrier, respective ones of said plurality of said signal pads electrically coupled to respective ones of said wire bond fingers;

a first ground plane generally covering said top side of said carrier, said first ground plane leaving said wire bond fingers exposed for interconnection with the bond wires;

a second ground plane covering a central area of said bottom side of said carrier,

said signal pads on said bottom side generally arrayed around said second ground plane;

a plurality of thermal vias positioned within said mounting area and extending through said carrier to electrically and thermally couple said first and second ground planes; and

a plurality of ground pads on said bottom side of said carrier, said plurality of ground pads positioned within an area defined by said second ground plane and electrically coupled to said second ground plane.

14. The chip scale package carrier of claim 13 wherein said first ground plane comprises a hatched portion substantially covering said die mounting area on said top side of said carrier.

15. The chip scale package carrier of claim 14 wherein said thermal vias are positioned within said first ground plane and are generally arrayed around said hatched portion of said first ground plane.

16. The chip scale package carrier of claim 13 further comprising an electrical connection between the at least one ground connection of the die and said first ground plane.

17. The chip scale package carrier of claim 13 further comprising a plurality of signal vias providing said electrical coupling between said plurality of wire bond fingers and said signal pads.

18. The chip scale package carrier of claim 17 wherein respective ones of said plurality of signal vias correspond to respective ones of said plurality of wire bond fingers, said plurality of wire bond fingers arranged in groups with said corresponding ones of said plurality of signal vias, each one of said groups generally arrayed along a top-side edge of said carrier.

19. The chip scale package carrier of claim 18 wherein said first ground plane comprises a continuous metal plane completely surrounding each said group of said wire bond fingers and said corresponding signal vias.

20. The chip scale package carrier of claim 19 wherein a border defined by said first ground plane completely surrounding each said group of said wire bond fingers and said corresponding signal vias comprises a contoured border substantially following the contours of each said group.

21. The chip scale package of claim 13 further comprising a plurality of solder balls, respective ones of said solder balls attached to corresponding ones of said signal and ground pads, said plurality of solder ball pads providing for attachment of said carrier to the primary circuit board.

22. A carrier for interconnecting an integrated circuit die with a circuit board, comprising:

a) a substrate having a top surface;

b) a plurality of signal points disposed on the top surface of the substrate for interfacing with the integrated circuit die;

c) the plurality of signal points being disposed in groups with each group of

signal points being spaced from an adjacent group; and

d) a ground plane disposed generally around each of the groups of signal points and extending over a substantial area of the top surface of the substrate, the ground plane operative to ground the integrated circuit die.

23. The carrier of claim 22 wherein each group of signal points is completely bounded by a perimeter formed by the termination of the ground plane.

24. The carrier of claim 23 wherein the ground plane includes a central area and wherein the groups of signal points lie outwardly of and around the central area of the ground plane.

25. The carrier of claim 24 wherein the carrier assumes a generally rectangular shape having four edges and wherein there is provided four groups of signal points with each group being disposed adjacent one edge of the carrier.

26. The carrier of claim 22 wherein the ground plane includes a central portion having a series of openings formed therein.

27. The carrier of claim 26 wherein the central portion of the ground plane assumes a hatched configuration.

28. The carrier of claim 22 wherein respective signal points within each group includes a wire bond finger, and wherein respective wire bond fingers are connected to signal vias that extend through the substrate.

29. The carrier of claim 22 further including a series of thermal vias disposed inwardly of the groups of signal points and which are operative to transfer heat from the integrated circuit die through the substrate.

30. The carrier of claim 29 wherein the thermal vias also function as ground vias.

31. The carrier of claim 22 wherein the ground plane includes a central mounting area for receiving the integrated circuit die, and wherein the groups of signal points lie outwardly of and around the integrated circuit die when the integrated circuit die is mounted on the carrier.

32. The carrier of claim 22 including at least four groups of signal points with two of the groups lying in parallel relationship to each other.

33. The carrier of claim 22 wherein each group of signal points includes at least two rows of signal vias and a connector connected to each signal via.

34. The carrier of claim 33 wherein the two rows of signal vias are disposed in parallel relationship and wherein the connectors connected to the vias are also disposed in parallel relationship.

35. The carrier of claim 34 wherein the signal vias of each row within each group of signal points are offset with respect to the adjacent row.